REMARKS

This Amendment seeks to place this application in condition for allowance. All of the Examiner's rejections have been addressed. Several of the pending claims have been amended. No new matter has been added.

OFFICE ACTION

In the office Action mailed August 1, 2000, the Examiner rejected claims 151-179 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art. Furthermore, the Examiner determined that the instant application is not obvious in view of U.S. Patent 6,034,214 (hereinafter "the '214 patent"), the parent to the instant application. Should the Examiner change his position, Applicants would submit a terminal disclaimer to overcome such a rejection.

Rejection - 35 U.S.C. § 112:

Applicants respectfully disagree with the Examiner's rejection that the claims contain subject matter not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. Here, the Examiner stated that the specification does not provide support for the limitations directed to "providing first and second portions of a first amount of data synchronous with external clock signal transitions." Each rejection will be addressed separately below.

Claim 151:

Claim 151 is directed to a method of controlling a memory device. The specification on page 13, lines 13-17, page 20, lines 24-25, and page 21, lines 18-20, and Figures 2 and 3, describe and illustrate a master 11 (e.g., a CPU or bus controller) controlling a memory device 13. In a write operation, the master issues a write request to the memory device, and in response to the write request, the memory device inputs a first amount of data corresponding to first block size information. In one embodiment, input receiver 71 (see, Figure 10) samples a first portion of the data at time 127 (see, Figure 13) and input receiver 72 (see, Figure 10) samples a second portion of the data at time 125 (see, Figure 13). In this regard, the specification on page 58, lines 18-21 states:

> The complement internal device clock is used to clock the 'even' input receivers to sample at time 127, while the true internal device clock is used to clock the 'odd' input receivers to sample at time 125.

Claim 151 requires, in part:

> providing a first portion of the first amount of data to the memory device synchronously with respect to a first transition of an external clock signal, and a second portion of the first amount of data synchronously with respect to a second transition of the external clock signal.

In one embodiment, the device interface of the master includes, among other things, an electrical interface which includes input/output circuitry, i.e., input receivers and bus drivers. (see, page 53, line

5-7). "A block diagram of the preferred input/output circuit ... is shown in Figure 10." (page 53, lines 24-25). In this embodiment, the input/output circuitry "consists of a set of input receivers 71, 72 and output driver 76." (page 54, lines 3-4).[1]

The output driver (76 in Figure 10) provides a first portion of the data to the memory device (via the bus) synchronously with respect to a falling edge of the complement internal device clock 74 (CLK\ of Figures 10 and 13) and provides a second portion of the data to the memory device synchronously with respect to a falling edge of the true internal device clock 73 (CLK of Figures 10 and 13). In this regard, the specification on page 58 lines 21-25 (emphasis added) states:

> The true and complement internal device clocks are also used to select which data is driven to the output drivers. The gate delay between the internal device clock and output circuits driving the bus is slightly greater than the corresponding delay for the input circuits ....

Thus, the specification, as filed, describes that the output driver (76 in Figure 10) outputs data onto the bus synchronously with respect to falling edges of the true and complement internal device clocks (73 and 74 in Figures 10 and 13). A first portion of the data is output synchronously with respect to the falling edge of the complement

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[1] The specification at page 53, line 25 to page 54, line 8 states that (emphasis added):

> [The input/output] circuitry is particularly well-suited for use in DRAM devices but it can be used or modified by one skilled in the art for use in other devices connected to the bus of this invention. It consists of a set of input receivers 71, 72 and output driver 76 connected to input/output line 69 and pad 75 and circuitry to use the internal clock 73 and internal clock complement 74 to drive the input interface. The clocked input receivers take advantage of the synchronous nature of the bus.

internal device clock and a second portion of the data is output synchronously with respect to the falling edge of the true internal device clock.

In one embodiment, the true and complement internal device clocks are generated using an external clock and a delay lock loop circuit (see, page 57, lines 3-25).[2] The internal device clocks are synchronized with transitions (e.g., rising and falling edges) of the external clock. (see, page 58, line 1 to line 18 and Figure 13). Thus, in one embodiment, data is provided onto the bus synchronously with respect to a first and a second transition of the external clock, via output driver 76 and internal device clocks 73 and 74. (see, Figures 10 and 13 and page 58 lines 21-23 and page 53, line 25 to page 54, line 8).

In sum, Applicants submit that every feature of claim 151 is fully supported by the application as filed.

Claim 163:

Claim 163 recites a method of operation of a memory device. Claim 163 recites, among other things:

> sampling a first portion of the first amount of data synchronously with respect to a first transition of an external clock signal and a second portion of the first amount of data synchronously with respect to a second transition of the external clock signal.

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[2] It should be noted that "[b]us clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks." Specification, page 46, line 23 to page 47, line 1.

In one embodiment, input receiver 71 (see, Figure 10) samples a first portion of the data at time 127 (see, Figure 13) and input receiver 72 (see, Figure 10) samples a second portion of the data at time 125 (see, Figure 13). In this regard, the specification on page 58, lines 18-21 states:

> The complement internal device clock is used to clock the 'even' input receivers to sample at time 127, while the true internal device clock is used to clock the 'odd' input receivers to sample at time 125.

In one embodiment, the internal device clocks are generated by a delay lock loop using an external clock (see, Page 57, lines 3-25) to synchronize internal device clocks 73 and 74 with the external clock via delay adjustment of the internal device clocks 73 and 74. Since the true and complement internal device clocks are synchronized with the external clock, data is sampled synchronously with respect to the external clock.[3] Thus, in one embodiment, data is sampled synchronously with respect to a first and a second transition of the external clock, via input receivers 71 and 72 and internal device clocks 73 and 74. (see, Figures 10 and 13 and page 58 lines 18-21 and page 54, lines 3-12).

Applicants submit that every feature of claim 158 is fully supported by the application as filed.

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[3]It should be noted that "[b]us clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks." Specification, page 46, line 23 to page 47, line 1.

Claim 174:

Claim 174 recites a method of operation of an integrated circuit device. Claim 174 recites, among other things:

> sampling a first portion of the amount of data synchronously with respect to a first transition of an external clock signal and a second portion of the amount of data synchronously with respect to a second transition of the external clock signal ....

The integrated circuit device samples an amount of data, the amount of data being defined by block size information. In one embodiment, input receiver 71 (see, Figure 10) samples a first portion of the data at time 127 (see, Figure 13) and input receiver 72 (see, Figure 10) samples a second portion of the data at time 125 (see, Figure 13). In this regard, the specification on page 58, lines 18-21 states:

> The complement internal device clock is used to clock the 'even' input receivers to sample at time 127, while the true internal device clock is used to clock the 'odd' input receivers to sample at time 125.

In one embodiment, the internal device clocks are generated by a delay lock loop using an external clock (see, Page 57, lines 3-25) to synchronize internal device clocks 73 and 74 with the external clock via delay adjustment of the internal device clocks 73 and 74. (see the time relationships illustrated by the dotted lines in Figure 13). Since the true and complement internal device clocks are synchronized with the external clock, data is sampled synchronously with respect to the external clock. Thus, in one embodiment, data is sampled synchronously with respect to a first and a second transition of the external clock, via input receivers 71 and 72 and internal device

clocks 73 and 74. (see, Figures 10 and 13 and page 58 lines 18-21 and page 54, lines 3-12).

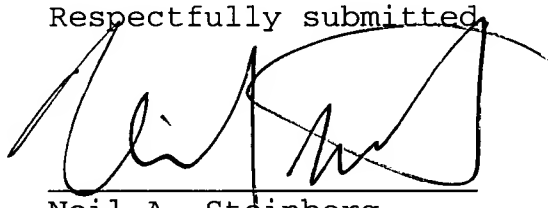
Applicants submit that every feature of claim 174 is fully supported by the application as filed.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 650-944-7772.

Respectfully submitted,



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